

## Section I. (Amended Claims)

Amend claim 27 as set out below in the listing of pending claims 1-39.

1. (Previously presented): A microelectronic structure comprising:

at least one layer of high dielectric constant material;

at least one conductive barrier layer in contact with the layer of high dielectric constant material, wherein such conductive barrier layer comprises at least one material selected from the group consisting of Pt, Ir, IrO<sub>2</sub>, Ir<sub>2</sub>O<sub>3</sub>, Ru, RuO<sub>2</sub>, TaN, NbN, HfN, ZrN, WN, W<sub>2</sub>N, TiAlN, TaSiN, NbAlN, and compatible combinations, mixtures and alloys thereof;

at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises metal or metal alloy including a material selected from the group consisting of Cu and Al;

wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;

wherein when said material of said at least one metal layer is Al, said at least one material of said conductive barrier layer is not Ir or IrO<sub>2</sub>.

2. (Previously presented): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises at least one material selected from the group consisting of TaN, NbN, HfN, ZrN, WN, W<sub>2</sub>N, TiAlN, TaSiN, and NbAlN.

3. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises TiAlN.

4. (Original): A microelectronic structure according to claim 1, wherein said metal layer comprises Cu or Cu alloy.

5. (Original): A microelectronic structure according to claim 1, wherein said metal layer comprises Al or Al alloy.
6. (Original): A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises a complex metal oxide selected from the group consisting of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  (SBT),  $(\text{Ba,Sr})\text{TiO}_3$  (BST),  $\text{BiTaO}_4$  (BT), and  $\text{Pb}(\text{Zr,Ti})\text{O}_3$  (PZT).
7. (Original): A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises perovskite BST material.
8. (Original): A microelectronic structure according to claim 1, wherein said layer of high dielectric constant material comprises amorphous BST material.
9. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 1nm to about 100nm.
10. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer has a thickness in a range of from about 5nm to about 20nm.
11. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Pt.
12. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ir.
13. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises  $\text{IrO}_2$ .
14. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises Ru.

15. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises  $\text{RuO}_2$ .
16. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises  $\text{TiAlN}$ .
17. (Original): A microelectronic structure according to claim 1, wherein said conductive barrier layer comprises  $\text{TaN}$ .
18. (Original): A microelectronic structure according to claim 1, comprising a first conductive barrier layer and a second conductive barrier layer, wherein the first conductive barrier layer is in contact with the layer of high dielectric constant material, and the second conductive barrier layer overlies said first conductive barrier layer and is in contact with the metal layer.
19. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises  $\text{IrO}_2$ .
20. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises  $\text{TiAlN}$ .
21. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Pt, and said second conductive barrier layer comprises Ir.
22. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises  $\text{IrO}_2$ .
23. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises Ir, and said second conductive barrier layer comprises  $\text{TiAlN}$ .

24. (Original): A micro electronic structure according to claim 18, wherein said first conductive barrier layer comprises  $\text{IrO}_2$ , and said second conductive barrier layer comprises Ir.
25. (Original): A microelectronic structure according to claim 18, wherein said first conductive barrier layer comprises  $\text{IrO}_2$ , and said second conductive barrier layer comprises TiAlN.
26. (Original): A microelectronic structure according to claim 1, comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer.
27. (Currently amended): A microelectronic structure according to claim 26 comprising:
- at least one layer of high dielectric constant material;
- at least one conductive barrier layer in contact with the layer of high dielectric constant material;
- at least one metal layer in contact with the conductive barrier layer, wherein said metal layer comprises Cu or Cu alloy;
- wherein said at least one conductive barrier layer is between said at least one layer of high dielectric constant material and said at least one metal layer;
- said at least one conductive barrier layer comprising a first conductive barrier layer, a second conductive barrier layer, and a third conductive barrier layer, wherein said first conductive barrier layer is in contact with the layer of high dielectric constant material, said second conductive barrier layer overlies said first conductive barrier layer, and said third conductive barrier layer overlies said second conductive barrier layer and is in contact with the metal layer,

wherein said first conductive barrier layer comprises  $\text{IrO}_2$ , said second conductive barrier layer comprises  $\text{Ir}_2\text{O}_3$ , and said third conductive barrier layer comprises Ir.

28. (Original): A microelectronic structure according to claim 1, comprising:

at least one layer of perovskite BST material;

a first conductive barrier layer in contact with the layer of perovskite BST material, and comprising Pt;

a second conductive barrier layer overlaying said first conductive barrier layer, and comprising Ir; and

at least one metal layer in contact with said second conductive barrier layer, comprising Cu or Cu alloy.

29. (Original): A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous BST material;

a conductive barrier layer in contact with the layer of amorphous BST material, comprising at least one material selected from the group consisting of Ir, Ru,  $\text{RuO}_2$ , and  $\text{IrO}_2$ ;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

30. (Previously presented): A microelectronic structure according to claim 1, comprising:

at least one layer of amorphous SBT material;

a conductive barrier layer in contact with the layer of amorphous SBT material, comprising at least one material selected from the group consisting of Ir, Ru, TaN and TiAlN;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

31. (Original): A microelectronic structure according to claim 1, comprising:

at least one layer of PZT material;

a conductive barrier layer in contact with the layer of PZT material, comprising at least one material selected from the group consisting of Ir, Ru, RuO<sub>2</sub>, and IrO<sub>2</sub>;

at least one metal layer in contact with the conductive barrier layer, comprising Cu or Cu alloy.

32. (Original): A microelectronic structure according to claim 1, comprising a capacitor structure selected from the group consisting of stack capacitors and trench capacitors.

33. (Original): A microelectronic structure according to claim 1, comprising a memory cell integrated circuit structure.

34. (Original): A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a non-volatile memory cell integrated circuit structure.

35. (Original): A microelectronic structure according to claim 33, wherein the memory cell integrated circuit structure comprises a dynamic random access memory cell integrated circuit structure.

36. (Original): A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises a decoupling circuit.

37. (Original): A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an impedance matching circuit.

38. (Original): A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an analog circuit component.
39. (Original): A microelectronic structure according to claim 1, wherein the integrated circuit structure comprises an active circuit element selected from the group consisting of electrically tunable capacitor, sensor, and microelectromechanical machine MEMS).